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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/624,596 | 07/23/2003 | Yoshihisa Matsubara | 8020-1021-1 | 7618 |

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YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

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| EXAMINER |
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PERALTA, GINETTE

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| ART UNIT | PAPER NUMBER |
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2814

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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|------------------------------|--------------------------------------|---------------------------------------------|--|
| Office Action Summary | Application No. 10/624,596 | Applicant(s) MATSUBARA, YOSHIHISA | |
| | Examiner Ginette Peralta | Art Unit 2814 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/290259.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>7/23/03</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ting et al. (U. S. Pat. 5,969,422) in view of Blish, II et al. (U. S. Pat. 5,882,738) and Doan et al. (U. S. Pat. 5,372,974).

Ting et al. teaches a method for manufacturing a semiconductor device that has a substrate with an interlayer insulation film thereon, the interlayer insulation film having therein a contact hole, a via hole and a trench for a plug electrode and a buried wiring; wherein the contact hole, via hole or trench is lined with a barrier film 30 made of tantalum, and an amorphous metal film 14 comprising a refractory metal that may be tantalum and copper; wherein the contact hole, via hole or trench is filled with a copper based conductive material 15 to form a plug electrode or buried wiring; and the amorphous metal film is between the barrier metal film and the copper based material; the method comprising the steps of preparing a semiconductor substrate, formed in which is the interlayer insulation film provided with the contact hole, via hole or trench, as shown in fig. 4; forming the tantalum-base barrier film 30 in the contact hole, via hole

or trench, as shown in fig. 3, and forming the copper based conductive film on the tantalum base barrier film.

Ting et al. shows all the disclosed features of the claim with the exception of the tantalum oxide film lining the contact hole, via hole or trench and being in between the interlayer insulation film and the barrier layer; and heat-treating the semiconductor substrate with the tantalum-base barrier film and the copper-base conductive film in a non-oxidizing atmosphere.

Blish, II et al. discloses a method of forming a metallization layer in a semiconductor structure that includes forming a tantalum-base barrier film; forming the aluminum or copper-based conductive film on the tantalum-base barrier film; and heat-treating the semiconductor substrate with the tantalum-base barrier film and the copper-base conductive film in a non-oxidizing atmosphere, wherein the structure is subjected to a heat treatment after the deposition of the tantalum-base barrier film and the copper-based conductive film for the disclosed intended purpose of improving electromigration performance characteristics in an interconnection in a semiconductor device.

Doan et al. shows a semiconductor device that comprises a tantalum oxide layer between an insulating film 80 and a second layer comprising tantalum, wherein the tantalum oxide layer and the tantalum layer form layer 85 of Fig. 7, and the layers are used for the disclosed intended purpose of forming a barrier layer between copper and the insulating layer and enabling the layers to uniformly reflow during a heating step.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to heat treat the structure as Blish, II et al. discloses and to use a tantalum oxide layer between the insulating layer and the barrier layer, for the disclosed intended purpose of improving electromigration performance characteristics in an interconnection in a semiconductor device. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that an amorphous film comprising tantalum and copper will form at the interface of the tantalum base film and the copper base film.

Regarding claim 2, Blish, II et al. discloses that the heat-treating step is performed at a temperature of 450°C. It would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the temperature of the heat treatment between 400 to 700° as there is no statement denoting the criticality of the temperature range, and the values taught by Blish, II et al. lie within the claimed range.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ting et al. in view of Blish, II et al. and Doan et al. as applied to claims 1 and 2 above, and further in view of Dubina (U. S. Pat. 6,077,780).

Ting et al. as modified by Blish, II et al. and Doan et al. discloses the claimed invention with the exception of forming the copper based conductive layer by using a first step of forming a copper based thin film on the tantalum-base barrier film, and a second step of forming a copper based thick film on the copper based thin film.

Dubina discloses a method of forming a semiconductor device that comprises having a substrate with an interlayer insulation film 554 thereon, the interlayer insulation film having therein a contact hole, or a trench for a plug electrode or buried wiring; wherein the contact hole, or trench is lined with a barrier film 556 made of tantalum, and a metal film 558 comprising a refractory metal that may be tantalum and copper; wherein the contact hole or trench is filled with a copper based conductive material 652 to form a plug electrode or buried wiring; and the metal film 558 is between the barrier metal film 556 and the copper based material 652; the method comprising the steps of preparing a semiconductor substrate, formed in which is the interlayer insulation film provided with the contact hole, via hole or trench; forming the tantalum-base barrier film 556 in the contact hole, via hole or trench, and forming the copper based conductive film on the tantalum base barrier film; wherein the copper based conductive layer is formed by using a first step of forming a copper based thin film on the tantalum-base barrier film, and a second step of forming a copper based thick film on the copper based thin film, wherein this two step process is used for the disclosed intended purpose of minimizing voids and seams that may occur in openings of high aspect ratios, and minimizing electromigration failures.

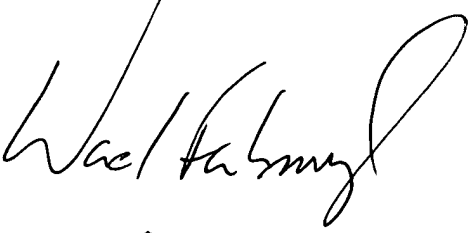
Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the copper-based conductive layer by the two step process taught by Dubina for the disclosed intended purpose of minimizing voids and seams that may occur in openings of high aspect ratios, and minimizing electromigration failure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571)272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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